DIGITAL ELECTRONICS

QUESTION BANK

Section A:

1. Which of the following are analog quantities, and which are digital?

(a) Number of atoms in a simple of material

(b) Altitude of an aircraft

(c) Pressure in a bicycle tire

2. Convert the following binary numbers to their equivalent decimal values.

(a) 110012 =_____10

(b) 1001.1001

(c) 10011011001.10110

3. Using 3 bits, show the binary counting sequence from 000 to 111.

4. What is the maximum number that we can count upto using 10 bits?

5. How many bits are needed to count upto a maximum of 511?

6. Suppose that the decimal integer values from 0 to 15 are to be transmitted.(a) How many lines will be needed if parallel representation is used?

(a) How many miles will be needed if parallel representation is used?

(b) How many will be needed if serial representation is used?

7. Convert each of the following decimal numbers to octal.
(a) 59 (b) 65536
(c) 255 (d) 919

8. Convert each of the following octal numbers to decimal.
(a) 57 (b) 65536
(c) 255 (d) 1004

9.Convert these hex values to decimal(a) 92 (b) 2C0(c) 1A6 (d) 7FF(d) 37FD

10. Encode these decimal numbers in BCD(a) 47 (b) 1204(c) 187 (d) 962

11.Add the following in binary. Check result by doing addition in decimal.

(a) 1010 +1011
(b) 111+0011
(c) 1011.1101 +11.1
(d) 0.1011 + 0.1111
(e) 10011011 + 10011101

12. Represent each of the following signed decimal numbers in the 2's complement system. Use a total of 8 bits including sign bit.
(a) + 32 (e) -1
(b) -14 (f) -128
(c) +63 (g) +169

13. Each of the following numbers represents a signed decimal number in the 2's complement system. Determine the decimal value in each case.
(a) 01101 (e) 0111111
(b) 11101 (f) 100000
(c) 01111011 (g) 111111
(d) 10011001 (h) 1000001

Section B:

1. Write the truth table for a half adder (inputs A and B; outputs Sum and Carry). From the truth table design a logic circuit that will act as a half adder.

- 2. Define each of the following terms.
- (a) Full adder
- (b) 2's complement
- (c) Arithmetic-logic unit
- (d) Sign bit
- (e) Overflow
- (f) Accumulator
- (g) Parallel adder
- (h) Look-ahead carry
- (i) Negation
- (j) B-register

3. Simply the following expressions using Boolean algebra. (a) x = ABC + AC(b) y = (Q + R) (Q + R)(c) w = ABC + ABC + A(d) q = RST (R + S + T)(e) x = ABC + ABC + ABC + ABC + ABC(f) z = (B + C) (B + C) + A + B + C (g) y = (C+D) + ACD + ABC + ABCD + ACD

4. Design a logic circuit whose output is HIGH *only* when a majority of inputs A, *B* and *C* are LOW.

5. A 4-bit binary number represented as A3 A2 A1 A0, where A3 A2 A1, and A0 represent the individual bits with A0 equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.

6. Implement the expression z = D + ABC + AC using ANDs, ORs, and INVERTERs; then convert to all NAND gates.

7. Design a logic circuit that will allow input signal A to pass through to the output only when control input B is LOW while control input C is High otherwise, the output is LOW.

8. Design a circuit that will inhibit the passage of an input signal only when control inputs B, C and D are all HIGH; the output is to be HIGH in the inhibited condition.

9. Design a logic circuit that controls the passages of a signal A according to the following requirements:

a. Output X will equal A when control inputs B and C are the same.

b. X will remain HIGH when B and C are different.

Section C:

- 1. Difference between combinational and sequential circuits (def, block diagram, examples)
- **2.** Difference between synchronous and asynchronous sequential logic circuits (Def, block diagram and other differences).
- 3. Difference in latch and flip flop (Hint: definition, block diagram, circuit diagrtam, advantages, disadvantages)
- 4. What is flip flop? Explain different types of flip flops with truth table and diagram.
- 5. Conversion of flip flops SR into T, SR into JK and D into T.
- 6. Explain edge triggered and level triggered flip flop. (Hint: Clock, levels, edges, flip flop working, difference between clocked and unclocked flip flop, timing diagram using some input and then corresponding output using diff levels and edges).

- 7. Race around condition
- 8. Master slave SR flip flop.
- 9. Master slave JK flip flop
- 10. Excitation table of all flip flops.
- 11. Register, Different types of registers (SISO, SIPO, PIPO, PISO, bidirectional, universal).
- 12. Counters and Difference between Synchronous Counter, Asynchronous (Ripple) Counter.
- 13. Designing of Modulo 7 up Asynchronous (Ripple Counter) and mod -7 down synchronous counter (hint: Block diagram, no of states counted and thus no. of flip flops required, state table, state diagram, simplified expression, logical ckt, timing diagram)
- 14. Mod -10 or BCD Up/Down sync and async Counter
- 15. Explain Ring Counter and Johnson Counter

Section D:

1. What is the function of Memory ENABLE input?

2. Describe the internal structure of ROM for storing 4k bytes and having a square register array.

3. Brifly describe the function of row select decoder, column select decoder and output buffer in a ROM.

4. What is the difference between MROM and PROM.

5. What is the difference between EPROM and EEPROM? What are the advantages of EEPROM over EPROM? What are disadvantages of EEPROM?

6. Discuss some applications of ROMs.

7. (a) Which RAM uses flip flops?(b) Which RAM uses Capacitors?

8. Disadvantages of DRAM over Static RAM.

9. The capacity of $2K \ge 16$ PROM is to be expanded to $16k \ge 16$. Find the number of PROM chips required and the number of address lines in the expanded memory.

10. What is data rate buffer?

- 11. Differentiate between ROM and RAM.
- 12. What is magnetic core memory?
- 13. Name some secondary memory devices

14. A certain memory has a capacity of 16K X 32. How many words does is store? What is the number of bits per word? How many memory cells does it contain?

15. What is the capacity of a memory that has 16 address inputs, four data inputs, and four data outputs?

16. What are Hazards and what are its types? How can hazardfree combination**al** networks be formed?